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Description

[NON-VOLATILE MEMORY CELL AND FABRICATION THEREOF]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a semiconductor device and a method for fabricating the same. More particularly, the present invention relates to a non-volatile memory cell and a method for fabricating the same.

[0003] Description of the Related Art

[0004] Non-volatile memory devices that use charge-trapping mechanisms have been widely studied. An earlier trapping-type non-volatile memory device is the mirror-bit SONOS memory as described in US 5,768,192, which uses a nitride layer disposed between two oxide layers for charge storage. Since silicon nitride is an insulating material and the charges trapped in the nitride trapping layer are localized, two bits can be stored in one memory cell as

a hot charge injection mechanism used for programming.

[0005] Recently, a category of trapping-type non-volatile memory that uses isolated conductive nano-particles for charge storage has been proposed. For example, US 6,342,716 B1 and US 6,413,819 disclose a trapping-type non-volatile memory that uses isolated dot elements for charge storage. US 6,165,842 discloses a method that forms silicon nano-crystals for charge storage by etching a polysilicon layer. US 6,297,095 B1 discloses a method that forms silicon nano-crystals for charge storage with controlled LPCVD or UHVCVD. Besides, US 6,303,516 B1 discloses a method that forms fine metal particles for charge storage by using an antigen-antibody pair binding method. In addition, US 5,783,263 and 5,876,480 disclose other methods for making nano-crystals. US 5,783,263 discloses a method that forms metal nano-particles by using carbon arc discharge on a graphite rod packed with the same metal, alloy, or oxide of metal or alloy. US 5,876,480 discloses a method that forms metal nano-particles by reducing ions of the same metal with some catalytic metal ions that are carried by vesicles in a dispersion system.

[0006] To well control the electrical properties of a trapping-type

non-volatile memory that uses nano-particles for charge storage, good uniformity in density of the nano-particles is required. Unfortunately, the nano-particles made with any one of the aforementioned methods in the prior art have poor uniformity, and the electrical properties of the non-volatile memory cannot be well controlled.

SUMMARY OF INVENTION

[0007] In view of the forgoing, this invention provides a non-volatile memory cell that contains metal nano-particles with better uniformity for charge storage.

[0008] This invention also provides a method for fabricating a non-volatile memory cell The method uses thermal dissociation for forming metal nano-particles to improve the uniformity of the same.

[0009] The non-volatile memory cell of this invention comprises a substrate, a charge-trapping layer, a gate and a source/drain. The charge-trapping layer comprises an insulating layer and metal nano-particles contained therein, wherein the metal nano-particles are formed with thermal dissociation of an oxide of the same metal. The gate is disposed on the charge-trapping layer, and the source/drain is located in the substrate beside the gate.

[0010] The method for fabricating a non-volatile memory cell of

this invention is described as follows. A first insulating layer, a metal oxide layer and a second insulating layer are sequentially formed on a substrate. An annealing is performed to convert the metal oxide layer to a plurality of metal nano-particles with thermal dissociation, while the first insulating layer, the second insulating layer and the metal nano-particles together constitute a charge-trapping layer. A gate is formed on the charge-trapping layer, and then a source/drain is formed in the substrate beside the gate.

[0011] Moreover, in the method for fabricating a non-volatile memory cell of this invention, several metal oxide layers and insulating layers can be alternately formed on the second insulating layer after the second insulating layer is formed. The metal oxide layers will be converted to multi layers of metal nano-particles in the subsequent annealing step.

[0012] As mentioned above, the metal oxide layer(s) is (are) converted to one or multi layers of metal nano-particles with thermal dissociation in this invention. Since the metal nano-particles capable of storing charges are isolated from each other, two bits can be stored in one non-volatile memory cell of this invention as in the case of the

conventional SONOS memory device. Meanwhile, the uniformity of the nano-particles in this invention is better as compared with the prior art, and the electrical properties of the non-volatile memory can be well controlled.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] FIGs. 1-3 illustrate a process flow of fabricating a non-volatile memory cell in a cross-sectional view according to a preferred embodiment of this invention, wherein FIG. 3 illustrates the structure of the non-volatile memory cell.

[0016] FIGs. 4-5 illustrates a method for forming multi layers of metal nano-particles according to the preferred embodiment of this invention.

[0017] FIG. 6 illustrates a programming operation of the non-

volatile memory cell illustrated in FIG. 3.

[0018] FIG. 7 illustrates a reading operation of the non-volatile memory cell illustrated in FIG. 3.

[0019] FIG. 8 illustrates an erasing operation of the non-volatile memory cell illustrated in FIG. 3.

DETAILED DESCRIPTION

[0020] FIG. 3 illustrates the structure of a non-volatile memory cell in a cross-sectional view according to the preferred embodiment of this invention.

[0021] Referring to FIG. 3, the non-volatile memory cell comprises a substrate 100, a charge-trapping layer 140, a gate 150, and a source/drain 160. The substrate 100 is, for example, a p-type silicon substrate. The charge-trapping layer 140 is disposed on the substrate 100, comprising an insulating layer 110 and metal nano-particles 130 contained therein. The insulating layer 110 may comprise silicon oxide, Al_2O_3, HfO_2 or ZrO_2, while silicon oxide is more preferable. The metal nano-particles 130 are formed with thermal dissociation of an oxide of the same metal, and may comprise platinum (Pt), iridium (Ir), ruthenium (Ru) or hafnium (Hf), while platinum is more preferable because the temperature for thermal dissociation of platinum oxide is lower. The diameter of the

metal nano-particles 130 ranges from 1nm to 20nm, and the distance between two metal nano-particles 130 ranges from 1nm to 10nm. The gate 150 is disposed on the charge-trapping layer 140, and comprises a material such as doped polysilicon. The source/drain 160 is located in the substrate 100 beside the gate 150, and is doped with an n-type dopant such as phosphorous (P) or arsenic (As).

[0022] FIGs. 1-3 illustrate a process flow of fabricating a non-volatile memory cell in a cross-sectional view according to the preferred embodiment of this invention.

[0023] Referring to FIG. 1, a first insulating layer 110a, a metal oxide layer 120 and a second insulating layer 110b are sequentially formed on a substrate 100. The first insulating layer 110a is formed with a method such as reactive sputtering or thermal oxidation, the metal oxide layer 120 with a method such as reactive sputtering, and the second insulating layer 110b with a method such as reactive sputtering or chemical vapor deposition (CVD). The first and the second insulating layers 110a and 110b may comprise the same material or different materials, and each of them comprises, for example, silicon oxide, Al_2O_3, HfO_2 or ZrO_2, while silicon oxide is more preferable. The

metal oxide layer 120 comprises a material such as platinum oxide (PtO_x), iridium oxide, ruthenium oxide or hafnium oxide, while PtO_x ($x = 0.1-10$) is more preferable because the temperature for thermal dissociation of PtO_x is lower.

[0024] As the first/second insulating layer 110a/b comprises silicon oxide formed with reactive sputtering, a silicon target is used with argon and oxygen gas introduced. As the metal oxide layer 120 comprises PtO_x formed with reactive sputtering, a platinum target is used with argon and oxygen gas introduced, and the sputtering conditions are analogous as in the case of silicon oxide sputtering. For example, the substrate temperature is room temperature, the flow rates of argon and oxygen gas are 5 sccm and 15 sccm, respectively, and the sputtering pressure is 20 mTorr for both the SiO_x deposition and the PtO_x deposition, while the sputtering rate for depositing SiO_x is 3 nm/min, and that for depositing PtO_x is 2 nm/min.

[0025] Referring to FIG. 2, an annealing is performed to convert the metal oxide layer 120 to a plurality of metal nanoparticles 130 with thermal dissociation. The metal nanoparticles 130 and the first and the second insulating layers 110a and 110b (insulating layer 110) together consti-

tute a charge-trapping layer 140. The annealing is preferably under vacuum for preventing contamination. As the metal oxide layer 120 comprises PtO_x, the annealing can be conducted at 420°C for 60 minutes, for example. The diameter of the platinum nano-particles formed with thermal dissociation ranges from about 1nm to about 20nm, and the distance between two platinum nano-particles ranges from about 1nm to about 10nm.

[0026] Referring to FIG. 3, a gate 150 is then formed on the charge-trapping layer 140, and the charge-trapping layer 140 is also patterned after the gate 150 is finished, wherein the gate 150 comprises a material such as doped polysilicon. Thereafter, a source/drain 160 is formed in the substrate 100 beside the gate 150 with a method such as ion implantation. The source/drain 160 is doped with phosphorous (P) or arsenic (As).

[0027] Besides, the metal nano-particles in the insulating layer can be formed with multi layers for increasing the number of trapping sites or other purposes. A method for forming multi layers of metal nano-particles is illustrated in FIGs. 4-5.

[0028] Referring to FIGs. 4-5, several insulating layers 410 and metal oxide layers 420 are alternately formed on a sub-

strate 400 to constitute a multi-layer structure. Thereafter, an annealing is performed under the same conditions as mentioned above, and the metal oxide layers 420 are converted to multi layers of metal nano-particles 430 with thermal dissociation. The multi layers of metal nano-particles 430 and the insulating layers 410 together constitute a charge-trapping layer 440.

[0029] Operations of the Non-Volatile Memory Cell

[0030] FIGs. 6, 7 and 8 illustrate a programming operation, a reading operation and an erasing operation, respectively, of the non-volatile memory cell illustrated in FIG. 3.

[0031] Referring to FIG. 6, the non-volatile memory may be programmed with channel hot electron injection (CHEI) mechanism. As bit 1 is to be written to the memory cell, the gate 150 is applied with a high positive voltage, the source/drain 160a is grounded, and the source/drain 160b is applied with a sufficiently high voltage capable of inducing hot electrons in the channel near the source/drain 160b. The hot electrons are driven into the right edge of the charge-trapping layer 140 by the high positive voltage on the gate 150, and trapped in the metal nano-particles 130 therein. The trapped electrons will not move to the other metal nano-particles 130 because of

the isolation of the insulating layer 110. Analogously, bit 2 (not shown) can be written to the left edge of the charge-trapping layer 140 and trapped in the metal nano-particles 130 therein by grounding the source/drain 160b and applying a sufficiently high voltage to the source/drain 160a.

[0032] Referring to FIG. 7, a bit in the memory cell can be read in the reverse direction. That is, as bit 1 is to be read, the source/drain 160a is applied with a positive voltage and the source/drain 160b is grounded, so that the current in the channel flows in a reverse direction as compared with the case of programming bit 1. If there are electrons stored in bit 1, as shown in FIG. 7, the portion of the channel under bit 1 is not turned on, and the current in the channel is in a low level. If bit 1 has not been written (not shown), the portion of the channel under bit 1 can be turned on, and the current in the channel is in a high level. Analogously, bit 2 can be read in a direction that is reverse to the current direction in the programming operation thereof.

[0033] Referring to FIG. 8, the non-volatile memory cell may be erased with Fowler-Nordheim tunneling mechanism. In the erasing operation, the gate 150 is applied with a high

negative voltage, and the substrate 100 is grounded or applied with a positive voltage. With the electric field established between the gate 150 and the substrate 100, the electrons stored in both bit 1 and bit 2 are driven to the substrate 100 from the charge-trapping layer 140, so that the erasing operation is completed.

[0034] As mentioned above, the metal oxide layer is converted to metal nano-particles with thermal dissociation in this invention. Since the metal nano-particles capable of storing charges are isolated from each other, two bits can be stored in one non-volatile memory cell as in the case of the conventional SONOS memory. Meanwhile, the uniformity of the nano-particles in this invention is better as compared with the prior art, and the electrical properties of the non-volatile memory can be well controlled.

[0035] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention covers modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.